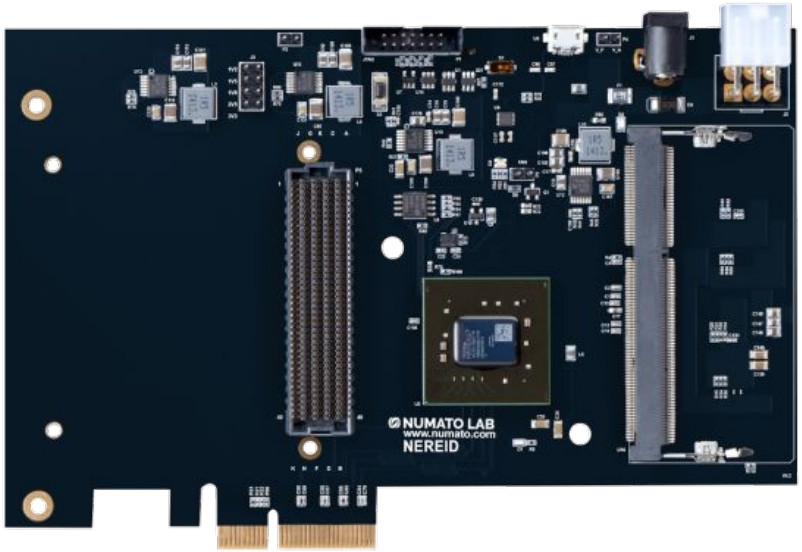
# PIONEER DAQ Development Progress

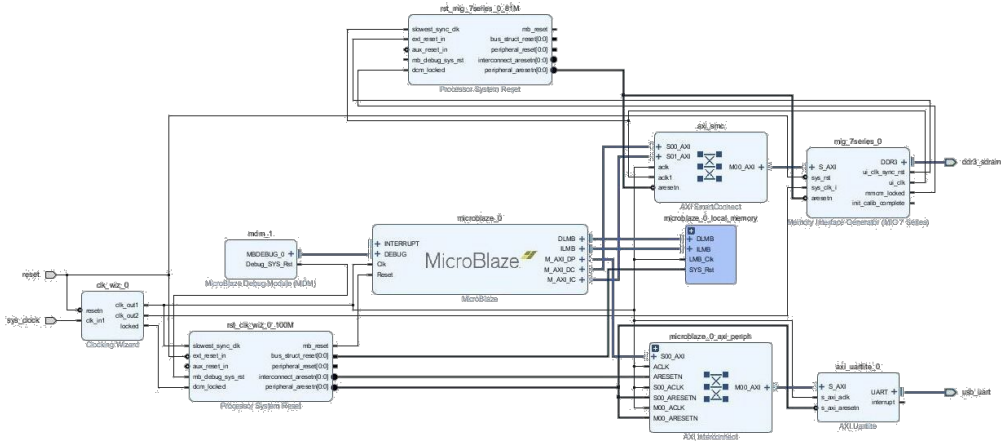
- Working with a few FPGA boards, mostly Nereid Kintex-7
- Can read and write configuration registers over PCIe
- Can generate and read fake data over UART
- Want to generate and read fake data over PCIe




**Nereid K7 PCI Express FPGA Development Board**

# PIONEER DAQ Development Outline

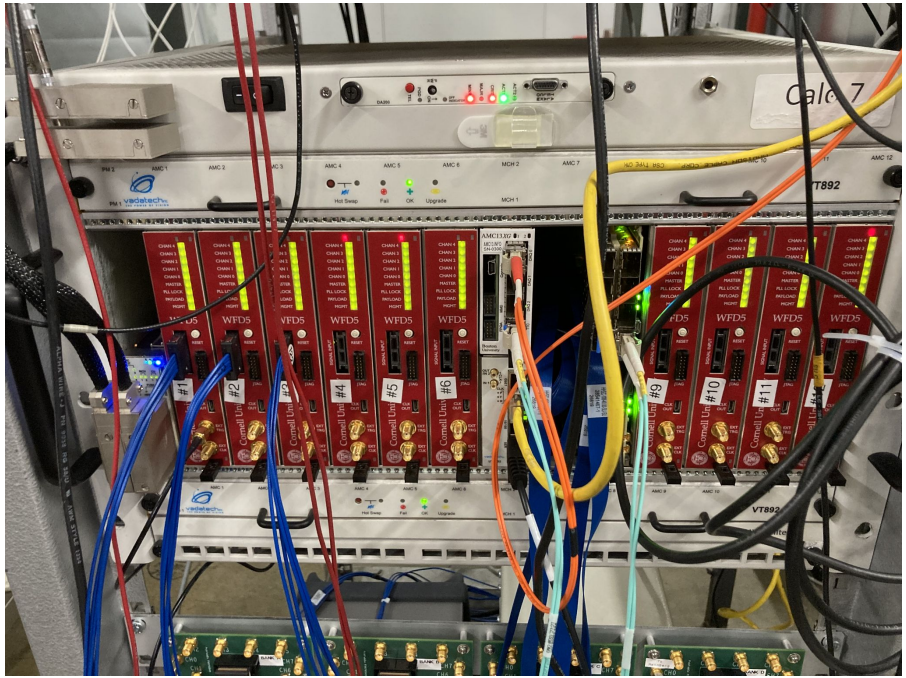
- Read and write FPGA configuration registers over PCIe
- Incorporate Microblaze processor, generate and transmit fake data over UART
- Generate and transmit fake data from FPGA over PCIe
- Create a C++ API for interfacing with FPGA over PCIe
- Add FMC ADC module to FPGA system
- Create Midas frontend incorporating PCIe FPGA communication
- Create similar design with HTG-K700 PCIe FPGA




**Microblaze with UART output Block Diagram**

# g-2 Modified DAQ Development Progress

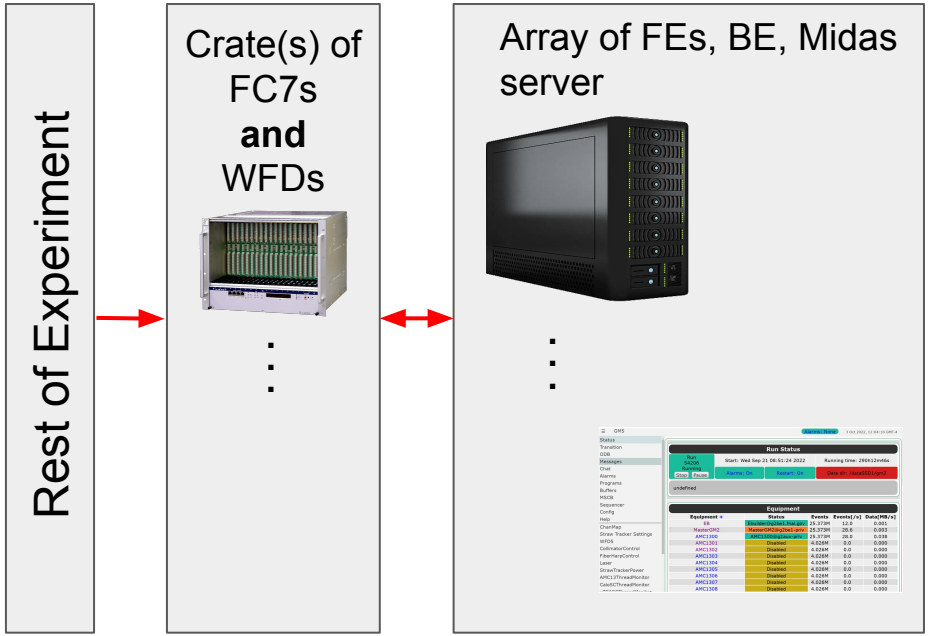
- In the process of building a “full” UKY teststand
- After some debugging, we have:
  - Established communication with our MCH module via 1GbE
  - Established communication with other modules via IPMI
  - Assigned IPs to other modules (AMC13, FC7, WFD5s)
- Waiting on ribbon cables for full setup




**Testbeam setup that we want to “duplicate”**

# g-2 Modified DAQ Development Outline

- Establish communication with all crate modules
- Finish hardware assembly
- Get frontend code running
- Debug (increase) rate capabilities by optimizing frontend code
- Add second crate to teststand




**Simplified DAQ Diagram**